



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

### PATENT APPLICATION

Applicant : Glenn J. Leedy

Application No.: 10/665,757 Confirmation No.: 6828

Filed : September 19, 2003

For : METHOD OF MAKING AN INTEGRATED

CIRCUIT (AS AMENDED)

Group Art Unit : 2822

Examiner : Pamela E. Perkins

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

# SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

#### Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97, applicant wishes to call the attention of the Examiner to the following documents:

	<u>U.S. Patents</u>	
Shibata	4,500,905	02/19/1985
Bergmans et al.	4,835,765	05/30/1989
Mauger et al.	4,919,749	04/24/1990
Wang, et al.	4,892,753	01/09/1990
Clements	4,897,708	01/30/1990
Kato, et al.	4,939,568	07/03/1990
Haisma et al.	4,983,251	01/08/1991
Wang, et al.	5,000,113	03/19/1991
Fueki et al.	5,144,142	09/01/1992
Linglain, et al.	5,240,458	08/31/1993
Bantien	5,259,247	11/09/1993
Fueki et al.	5,262,341	11/16/1993
Wang, et al.	RE 36,623	03/21/2000
Brix, et al.	6,087,284	07/11/2000
Lofgren et al.	6,230,233	05/08/2001
Brandes et al.	6,445,006	09/03/2002
Momohara	6,518,073	02/11/2003
Leedy	6,682,981	01/27/2004
Leedy	6,713,327	03/30/2004
RT71NES 00000036 10665757		

04/11/2005 MBIZUNES 00000036 10665757

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	Foreign Patents	
Germany	DE 32 33 195	03/17/1983
Japan	JP S60-126871	07/06/1985
Japan	JP S63-076484	04/06/1988
Japan	JP S63-229862	09/26/1988
EPO	EP 0 314 437	05/03/1989
Japan	JP H01-199476	08/10/1989
Japan	JP 03-127816	05/30/1991
Japan	JP 03-174715	07/29/1991
Japan	JP H03-284871	12/16/1991
PCT	WO 92/03848	03/05/1992
Japan	JP 04-076946	03/11/1992
Japan	JP 04-196263	07/16/1992
PCT	EP 0 518 283	12/16/1992
PCT	WO 01/05366	01/25/2001
PCT	WO 03/078305	09/25/2003

### Other Documents

Aboaf, J.A., "Stresses in  $SiO_2$  Films Obtained from the Thermal Decomposition of Tetraethylorthosilicate - Effect of Heat Treatment and Humidity," J. Electrochem. Soc.: Solid State Science; 116(12): 1732-1736 (Dec. 1969).

Scheuerman, R.J., "Fabrication of Thin Dielectric Films with Low Internal Stresses," J. Vac. Sci. and Tech., 7(1): 143-146 (1970).

Bailey, R., "Glass for Solid-State Devices: Glass film has low intrinsic compressive stress for isolating active layers of magnetic-bubble and other solid-state devices," NASA Tech Brief (1982).

"Partitioning Function and Packaging of Integrated Circuits for Physical Security of Data," IBM Technical Disclosure Bulletin, IBM Corp.; 32(1): 46-49 (June 1989).

Hsieh, et al., "Directional Deposition of Dielectric Silicon Oxide by Plasma Enhanced TEOS Process," 1989 Proceedings, Sixth International IEEE VLSI Multilevel Interconnection Conference, pp. 411-415 (1989).

Tessier, et al., "An Overview of Dielectric Materials for Multichip Modules," SPE, Electrical & Electronic Div.; (6): 260-269 (1991).

Treichel, et al., "Planarized Low-Stress Oxide/Nitride Passivation for ULSI Devices," J. Phys IV, Colloq. (France), 1 (C2): 839-846 (1991).

Krishnamoorthy, et al., "3-D Integration of MQW Modulators Over Active Submicron CMOS Circuits: 375 Mb/s Transimpedance Receiver -Transmitter Circuit," IEEE Photonics Technology Letters, 2(11): 1288-1290 (November 1995).

Tielert, et al., "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic," IEEE, XP-000704550, 121-124 (December 5, 1996).

"Miniature Electron Microscopes Without Vacuum Pumps, Self-Contained, Microfabricated Devices with Short Working Distances, Enable Operation in Air," NASA Tech Briefs, 39-40 (1998).

Sung, et al., "Well-aligned carbon nitride nanotubes synthesized in anodic alumina by electron cyclotron resonance chemical vapor deposition," Applied Physics Letters, Volume 74, Number 2, 197, 1999, January 11, 1999.

Partial European Search Report for Application No. EP 02009643 (October 8, 2002).

Phys. Rev., B, Condens, Matter Mater. Phys. (USA), Physical Review B (Condensed Matter and Materials Physics), 15 March 2003, APS through AIP, USA.

These documents are listed on the accompanying Form PTO-SB/08A (submitted in duplicate), and pursuant to 37 C.F.R. § 1.98(a)(2), copies of the non-U.S. Patent documents are enclosed herewith.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

Two of the references cited in this Supplemental Information Disclosure Statement (i.e., Bergmans et al. U.S. Patent 4,835,765 and Mauger et al. U.S. Patent 4,919,749) were cited in a communication from the U.S. patent office in a related U.S. application. In particular, these references were cited in the December 17, 2004 Office Action in applicant's related U.S. application No. 10/665,757. A copy of that Office Action is not enclosed herewith, as applicant assumes that it is readily available to the Examiner. However, if it is desirable for the Examiner to have the applicant provide the Office Action, applicant will do so on the request of the Examiner.

Two other references cited in this Supplemental Information Disclosure Statement (i.e., JP-127816 and JP-174715 (and its corresponding U.S. patents: Fueki et al. U.S. Patents 5,144,142 and 5,262,341)) were cited in a communication from a foreign patent office in a counterpart foreign application. In particular, these references were cited in the October 19, 2004 Office Action in applicant's corresponding Japanese application No. 2003-411658. A copy of that Office Action is also enclosed herewith.

An other of the references cited in this Supplemental Information Disclosure Statement (i.e., Lofgren et al. U.S. Patent 6,230,233) was cited in a communication from the U.S. patent office in a co-pending, commonly-assigned U.S. application. In particular, this reference was cited in the March 11, 2005 Office Action in U.S. application

No. 10/143,200. A copy of that Office Action is not enclosed herewith, as applicant assumes that it is readily available to the Examiner. However, if it is desirable for the Examiner to have the applicant provide the Office Action, applicant will do so on the request of the Examiner.

It is respectfully requested that this patent be:

(1) fully considered by the Patent and Trademark Office during the examination of this application; and (2) printed on any patent which may issue on this application. Applicant requests that a copy of Form PTO-SB/08A, as considered and initialed by the Examiner, be returned with the next communication.

This Statement is submitted after the mailing date of the first Office Action on the merits, but before the mailing date of any final office action under 37 C.F.R. § 1.113, a notice of allowance under 37 C.F.R. § 1.311, or an action that otherwise closes prosecution in the application. Pursuant to 37 C.F.R. § 1.97(c)(2), a check in the amount of \$180.00 in payment of the fee for submission of this Supplemental Information Disclosure Statement is transmitted herewith. The Director is hereby authorized to charge payment of any additional fees required in connection with this

Statement, or credit any overpayment of the same, to Deposit Account No. 06-1075. A duplicate copy of this Supplemental Information Disclosure Statement is enclosed herewith.

An early and favorable action is respectfully requested.

Respectfully submitted,

Jeffrey C. Aldridge

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Substitute for form 1449/PTO				Complete if known		
1				Application Number	10/665,757	
INF	ORMATION	DISC	LOSURE	Filing Date	September 19, 2003	
STATEMENT BY APPLICANT				First Named Inventor	Glenn J. Leedy	
31.	STATEMENT BY APPLICANT			Art Unit	2822	
(use as many sheets as necessary)				Examiner Name	Pamela E. Perkins	
Sheet	1	of	2	Attorney Docket Number	ELM-1 CONT.9	

U.S. PATENT DOCUMENTS					
Examiner initials*	Cite No.1	Document Number  Number – Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Documents	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		4,500,905	02/19/1985	Shibata	Figures Appear
		4,835,765	05/30/1989	Bergmans et al.	
		4,892,753	01/09/1990	Wang, et al.	
		4,897,708	01/30/90	Clements	
		4,919,749	04/24/1990	Mauger et al.	
		4,939,568	07/03/1990	Kato, et al.	
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		5,000,113	03/19/1991	Wang, et al.	
		5,144,142	09/01/1992	Fueki et al.	
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		RE 36,623	03/21/2000	Wang, et al.	
		6,087,284	07/11/2000	Brix, et al.	
		6,230,233	05/08/2001	Lofgren et al.	
		6,445,006	09/03/2002	Brandes et al.	
!		6,518,073	02/11/2003	Momohara	
		6,682,981	01/27/2004	Leedy	
		6,713,327	03/30/2004	Leedy	

	FOREIGN PATENT DOCUMENTS					
Examiner	Cite	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
initials	No.1	Country Code 1 - Number 2 - Kind Code 2		Applicant of Cited Documents		
•		DE 32 33 195 .	03/17/1983	Germany		
		JP S60-126871 `	07/06/1985	Japan		
		JP S63-076484 ·	04/06/1988	Japan		
		JP S63-229862	09/26/1988	Japan		
		EP 0 314 437	05/03/1989	EPO		
		JP H01-199476	08/10/1989	Japan		
		JP-03-127816	05/30/1991	Japan		
		JP-03-174715 -	07/29/1991	Japan	-	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered.

Include copy of this form with next communication to applicant.

Applicant's unique citation designation number (optional), See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. Applicant is to place a check mark here if English language translation is attached.

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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449/PTO			0	Complete if known		
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INFO	ORMAT	ON DIS	CLOSURE	Filing Date	September 19, 2003	
STATEMENT BY APPLICANT (use as many sheets as necessary)				First Named Inventor	Glenn J. Leedy	
			LIOAITI	Art Unit	2822	
			necessary)	Examiner Name	Pamela E. Perkins	
Sheet	2	of	2	Attorney Docket Number	ELM-1 CONT.9	

JP H03-284871 .	12/16/1991	Japan	
WO 92/03848 .	03/05/1992	PCT	
JP 04-076946 ·	03/11/1992	Japan	
JP-04-196,263	07/16/1992	Japan	
EP 0 518 283	12/16/1992	EPO	
WO 01/05366	01/25/2001	PCT	
WO 03/078305	09/25/2003	PCT	

		NON PATENT LITERATURE DOCUMENTS	
Examiner initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T <sup>6</sup>
_		Aboaf, J.A., "Stresses in SiO <sub>2</sub> Films Obtained from the Thermal Decomposition of Tetraethylorthosilicate – Effect of Heat Treatment and Humidity," J. Electrochem. Soc.: Solid State Science; 116(12): 1732-1736 (Dec. 1969).	
		Scheuerman, R.J., "Fabrication of Thin Dielectric Films with Low Internal Stresses," J. Vac. Sci. and Tech., 7(1): 143-146 (1970).	
		Bailey, R., "Glass for Solid-State Devices: Glass film has low intrinsic compressive stress for isolating active layers of magnetic-bubble and other solid-state devices," NASA Tech Brief (1982).	
		"Partitioning Function and Packaging of Integrated Circuits for Physical Security of Data," IBM Technical Disclosure Bulletin, IBM Corp.; 32(1): 46-49 (June 1989).	
		Hsieh, et al., "Directional Deposition of Dielectric Silicon Oxide by Plasma Enhanced TEOS Process," 1989 Proceedings, Sixth International IEEE VLSI Multilevel Interconnection Conference, pp. 411-415 (1989).	
-		Tessier, et al., "An Overview of Dielectric Materials for Multichip Modules," SPE, Electrical & Electronic Div.; (6): 260-269 (1991).	
		Treichel, et al., "Planarized Low-Stress Oxide/Nitride Passivation for ULSI Devices," J. Phys IV, Colloq. (France), 1 (C2): 839-846 (1991).	
		Krishnamoorthy, et al., "3-D Integration of MQW Modulators Over Active Submicron CMOS Circuits: 375 Mb/s Transimpedance Receiver –Transmitter Circuit," IEEE Photonics Technology Letters, 2(11): 1288-1290 (November 1995).	
		Tielert, et al., "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic," IEEE, XP-000704550, 121-124 (December 5, 1996).	
		"Miniature Electron Microscopes Without Vacuum Pumps, Self-Contained, Microfabricated Devices with Short Working Distances, Enable Operation in Air," NASA Tech Briefs, 39-40 (1998).	
		Sung, et al., "Well-aligned carbon nitride nanotubes synthesized in anodic alumina by electron cyclotron resonance chemical vapor deposition," Applied Physics Letters, Volume 74, Number 2, 197, 1999, January 11, 1999.	
		Partial European Search Report for Application No. EP 02009643 (October 8, 2002).	
		Phys. Rev., B, Condens, Matter Mater. Phys. (USA), Physical Review B (Condensed Matter and Materials Physics), 15 March 2003, APS through AIP, USA.	

Examiner Signature	Date	
Signature	Considered	
-		

All References Have Been Considered:	
	Examiner